

Application Serial No. 10/662,034

Attorney Docket No. 200309970-1

Claim 3 (currently amended). The computer system of claim 1,  
wherein:

the first FIFO buffer comprises means for receiving a plurality  
of bytes from the host processor; and

the send machine comprises means for transmitting the plurality  
of bytes over the ~~communications~~-system bus without interrupting the  
host processor.

Claim 4 (original). The computer system of claim 1, further  
comprising:

a receive machine coupled between the host processor and the  
bus controller; and

a second FIFO buffer coupled to the receive machine and coupled  
between the host processor and the bus controller.

Claim 5 (currently amended). The computer system of claim 4,  
wherein the receive machine comprises means for generating a message  
checksum for a message while the message is being received by the  
bus controller over the ~~communications~~-system bus.

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Claim 8 (currently amended). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the ~~communications-system~~ bus to the target device without obtaining the message again from the host processor if it is determined that the message was not received without errors by the target device.

Claim 9 (currently amended). The computer system of claim 1, further comprising:

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the ~~communications-system~~ bus after the ~~communications-system~~ bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

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Claim 10 (original). The computer system of claim 1, further comprising:

a byte timer coupled between the bus controller and the host processor.

Claim 11 (previously presented). The computer system of claim 10, wherein the byte timer comprises means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

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Claim 12 (currently amended). A computer system comprising:

a ~~communications~~-system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the ~~communications~~-system bus;

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the ~~communications~~-system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled between the host processor and the bus controller over ~~an~~-a first internal bus but not over the system bus, the first FIFO not being coupled to the send machine over the first internal bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the ~~communications~~-system bus without interrupting the host processor; and

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a second FIFO buffer coupled to the receive machine, the second FIFO further and coupled between the host processor and the bus controller over a second internal bus, the second FIFO but not being coupled to between the receive machine and the bus controller over the second internal bus but not over the system bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

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Claim 13 (currently amended). The computer system of claim 12, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the ~~communications-system~~ bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the ~~communications-system~~ bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the ~~communications-system~~ bus after the ~~communications-system~~ bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

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a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claims 14-41 (canceled)

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Claim 42 (currently amended). A computer system comprising:

a ~~communications-system~~ system bus;

a bus controller coupled to the ~~communications-system~~ system bus;

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the ~~communications-system~~ system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled between the host processor and the bus controller over an internal bus but not over the system bus, the first FIFO not being coupled to the send machine over the internal bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the ~~communications-system~~ system bus without interrupting the host processor;



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a second FIFO buffer coupled to the receive machine, the second FIFO further and coupled between the host processor and the bus controller over a second internal bus but not over the system bus, the second FIFO but not between being coupled to the receive machine and the bus controller over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

means for receiving a message from the host processor;

means for attempting to send the message over the communications system bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the communications system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the communications system bus after the communications system bus becomes available for use;

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a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

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Claim 43 (currently amended). A computer system comprising:

a ~~communications~~-system bus;

a bus controller coupled to the ~~communications~~-system bus;

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the ~~communications~~-system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled between the host processor and the bus controller over a first internal bus but not over the system bus, the first FIFO not being coupled to the send machine over the first internal bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the ~~communications~~-system bus without interrupting the host processor and means for generating a message checksum for a message while the message is being received by the bus controller over the ~~communications~~-system bus without interrupting the host processor; and

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a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over a second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

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Claim 44 (currently amended). A device for use in a computer system including a ~~communications~~system bus and a bus controller coupled to the ~~communications~~system bus, the device comprising:

a send machine coupled between a host processor and the bus controller, the send machine comprising means for transmitting the plurality of bytes over the ~~communications~~system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled between the host processor and the bus controller over a first internal bus but not over the system bus, the first FIFO not being coupled to the send machine over the first internal bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the ~~communications~~system bus without interrupting the host processor;

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a second FIFO buffer coupled to the receive machine, the first FIFO further coupled between the host processor and the bus controller over a second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

busfree count storage means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the ~~communications~~system bus after the ~~communications~~system bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.